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J. Douglas
8/24/01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	Atty. Docket
GERRIT J. KEESMAN	PHB 33,946C
Serial No. 08/901,338	Group Art Unit: 2615
Filed: July 28, 1997	Examiner: A. RAO

BUFFER MANAGEMENT IN VARIABLE BIT-RATE COMPRESSION SYSTEMS

Commissioner for Patents
Washington, D.C. 20231

Sir:

Transmitted herewith is a Reply Brief and two copies in the above-identified patent application.

Noted
8/27/01

Respectfully submitted,

By Cherie S. Werbel
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(914) 333-9605

CERTIFICATE OF MAILING

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Washington, D.C. 20231

On August 20 2001

By [signature]

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Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

REPLY BRIEF

Sir:

This Reply Brief is submitted in response to the Examiner's Answer mailed on June 19, 2001.

Appellant maintains the arguments submitted in the Brief on Appeal, mailed on March 30, 2001, and refutes the allegations made in the Examiner's Answer. In particular, Appellant respectfully refutes the allegation, on page 4, lines 6-10, that Kiriyama establishes an inverse relationship between the encoder buffer input rate (B1) and the bit-rate of the data stream leaving the decoder buffer (B2).

On pages 5-6 of his Answer the Examiner cites the three equations below in support of finding the inverse relationship.

(1) Sum Delay of encoder buffer memory = (B0) + (B1)

(2) Sum Delay of the decoder buffer delay = (B2) + (B3)

(3) [((B1) + (B0)) + ((B2) + (B3))] + "additional video delay" = THV where

B0 = delay associated with the encoder buffer input rate

B1 = delay associated with the encoder buffer output rate

B2 = delay associated with the decoder buffer output rate

B3 = delay associated with the decoder buffer input rate

Appellant wishes to point out, however, that the Examiner recited that B1 was the encoder buffer input rate on line 11 and line 19 of the Examiner's Answer but then assigned B1 as the encoder buffer output rate on page 6 line 6. Appellant believes this is an error and hereafter refers to B1 as the encoder buffer input rate and B0 as the encoder buffer output rate. Appellant also wishes to point out that in earlier Office Actions, the Examiner referred to B1 as the buffer input write in rate (see Office Action mailed 11/16/99 on page 3 line 11 stating "B1 is established as buffer input write in rate".) Now not only is the Examiner at times referring to B1 as the buffer output rate, but he also now assigns the variables B0-B3 to the delays associated with the rates instead of to the rates per se.

Appellant is going to proceed with the following definitions of the variables which were used on pages 4 and 5 of the Examiner's

Answer and assume that the definitions of B0 and B1 on page 6 of the Examiner's Answer are misstatements. Appellant is also going to refer to the variables B0-B3 as bit rates, and not "delays" associated with bit rates, as the only the term "rates" is recited in the language of Appellant's claims.

B1 = input rate to the encoder buffer

B0 = output rate of the encoder buffer

B3 = input rate to the video buffer

B2 = output rate of the video buffer

Appellant would like to take this opportunity to explain the error in the formulation of the Examiner's equations, which are the basis for what Appellant respectfully submits is the Examiner's flawed analysis. In stating that ED (the encoder delay) = B0 + B1, the Examiner oversimplifies the way that buffers work. A buffer can be analogized to a bucket of sand with a hole in the bottom. The bucket is filled at the top with an input rate of B1 and emptied by a hole in the bottom at an output rate of B0. Following the Examiner's equation, the amount of time a grain of sand stays in the buffer is represented by the sum of B0 and B1. Appellant respectfully submits that this is incorrect. The amount of time that a grain of sand remains in the bucket, i.e. its delay, depends not only on the instantaneous output rate, but also on how much

sand there is in the bucket in the first place. For example, if there is a lot of sand in the bucket, fresh sand at the top will be in the bucket longer, than if there were less sand in the bucket to begin with. The delay in the bucket is ultimately related then not just to the input and output rates but to these rates over time. Using the Examiner's notation, the encoder delay would be more correctly stated as ED = f((B0 + B1), t).

In any event, Appellant respectfully submits that ED = B0 + B1 is an incorrect simplification. If similarly simplified, the equation should be correctly stated as ED = B1 - B0. Buffer occupancy is determined by the difference between the buffer input rate (B1) and the buffer read out rate (B0). This is because as the hole in the sand bucket gets bigger, more sand flows out (B0 increases) and a particular grain of sand stays in the bucket a shorter period of time, i.e. the delay decreases.

Continuing with his interpretation of the flawed equations above, and as a result of manipulating the erroneous equation 3 on page 7, the Examiner concludes on page 8 that "[t]he fact that the slope of the -2 defines the mathematical equation (5) as an inverse relationship because of the negative slope". Applicant respectfully submits that because the formulation of equations 1, 2, and 3 are incorrect, this observation, whether or not correct, is irrelevant to establishing Kiriyama as prior art and does not demonstrate that Kiriyama discloses "deriving a second bit rate as a percentage of

the first bit rate, which percentage changes inversely in relation to changes in the first bit rate".

Appellant has included in Exhibit A, attached hereto, annotated drawings, which illustrate the differences between Kiriyama and the present invention. These drawings explain the relationships in Kiriyama that are disclosed in column 10, lines 17-19, which the Examiner expresses in equations, namely:

> "a sum delay of the delay in the buffer memory 39 of FIG. 5 plus the additional video delay becomes equal to a predetermined video delay threshold value THV. In this manner, the read video data are produced from the video buffer memory 71 with the sum delay relative to supply of the encoded video signal to the buffer memory 39"

Using the Examiner's method of notation, the encoder buffer delay is correctly expressed as ED = B1 - B0. The decoder buffer (71 above) delay is correctly expressed as VD = B3 - B2. According to the relationships quoted above, ED + VD = THV. Substituting for ED and VD gives B1 - B0 + B3 - B2 = THV. Assuming no data loss, B0 = B3 and therefore cancel. The resulting equation is B1 - B2 = THV. Accordingly, Appellant respectfully submits that Kiriyama does not disclose the inverse relationship between the encoder buffer input rate and the bit-rate of the data stream leaving the decoder buffer

that the Examiner asserts.

Wherefore, it is respectfully submitted that the rejections of claims 1-12 and 14 under 35 USC Section 102 are improper. Reversal of the rejections on appeal is respectfully requested.

Respectfully submitted,

By Cherie S. Werbel

Cherie S. Werbel, Reg. 40,870
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August 20, 2001

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On August 20 2001

By

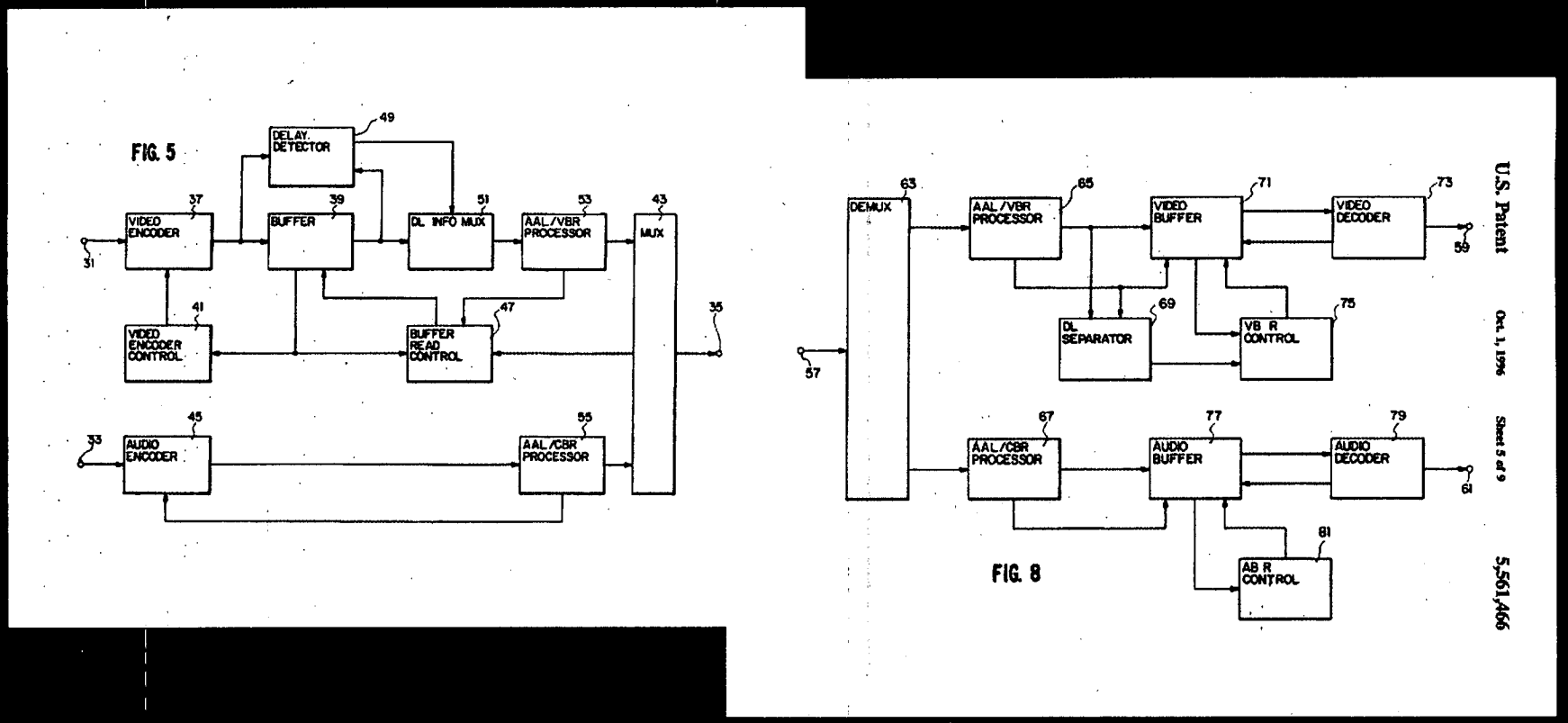
PHB 33946 US (Keesman)

Keesman in relation to US5561466 (Kiriyama)

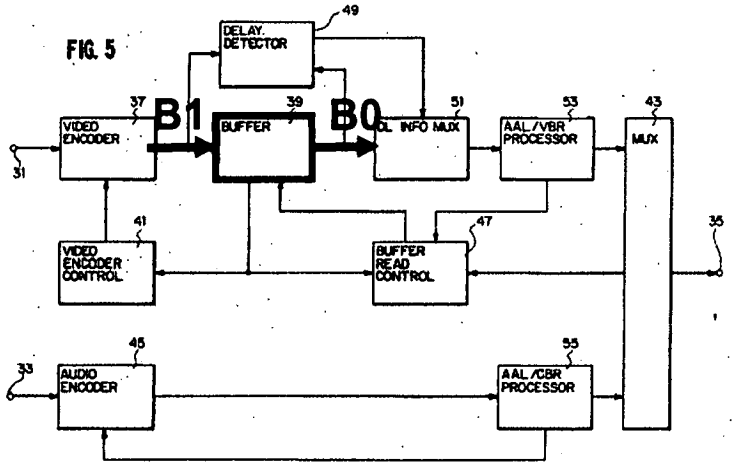
Let's make things better.

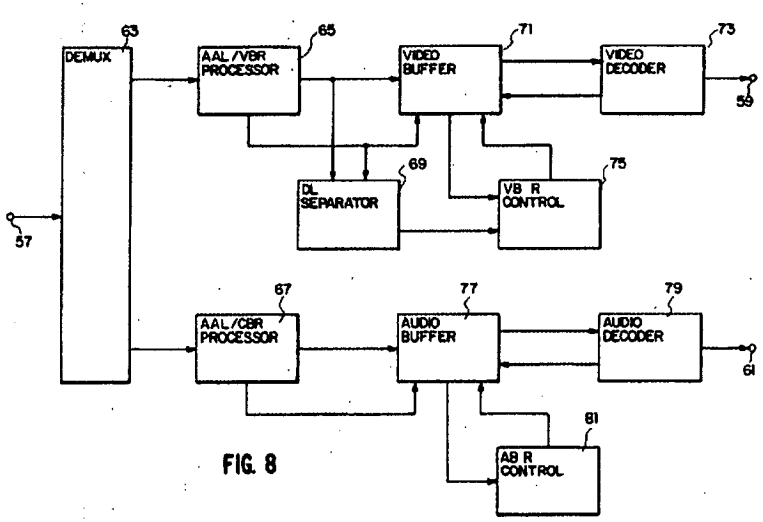
PHILIPS

These are figures 5 and 8 of Kiriyama which are an encoder & multiplexer / demultiplexer & decoder combination.



Superimposed in red are the portions of Keesman at issue. Using the examiner's definitions in the "examiner's answer" mailed 06/19/01, B1 is the bit rate at which data is written to the encoder buffer (line 8, page 4 of examiner's answer); and B0 is the bit rate at which data is read out the buffer (line 2, page 5 of examiner's answer). According to Keesman, changes in B0/B1 are inversely relates to changes in B0. The applicant admits that this relationship is met if changes in B1 are inversely related to changes in B0.

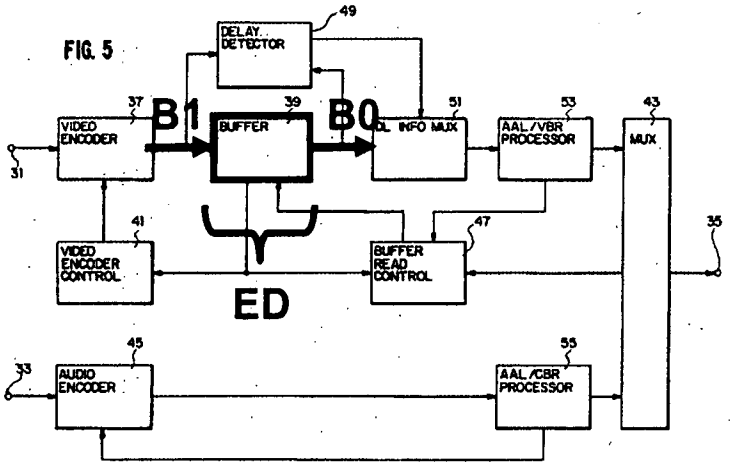




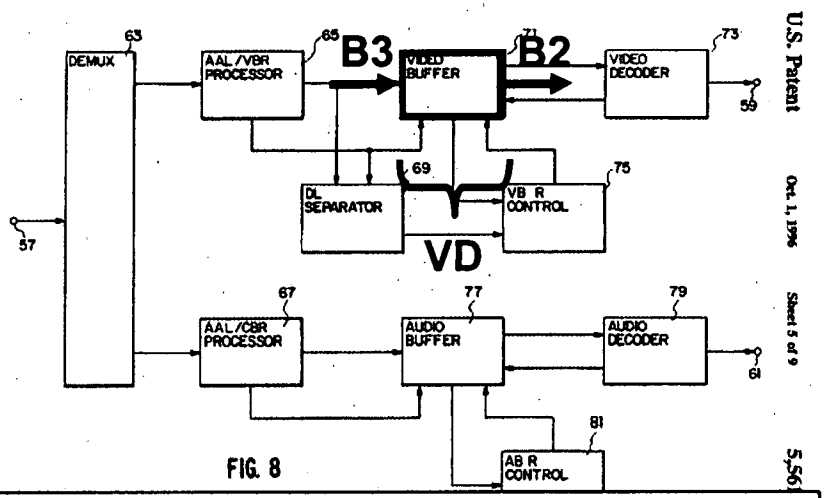
Let's make things better.

PHILIPS

Superimposed in blue is "condition 2" disclosed at lines 16 to 24 of column 10 of Kiriyama which states ED + VD = THV (constant). Both ED and VD are time delays measured in units of time. Following the examiner's definitions in the "examiner's answer" mailed 06/19/01, B2 is the bit rate at which data is read out the decoder buffer (line 21, page 4 of examiner's answer) and B3 is the bit rate at which data is written to the decoder buffer (line 22, page 4 of examiner's answer).

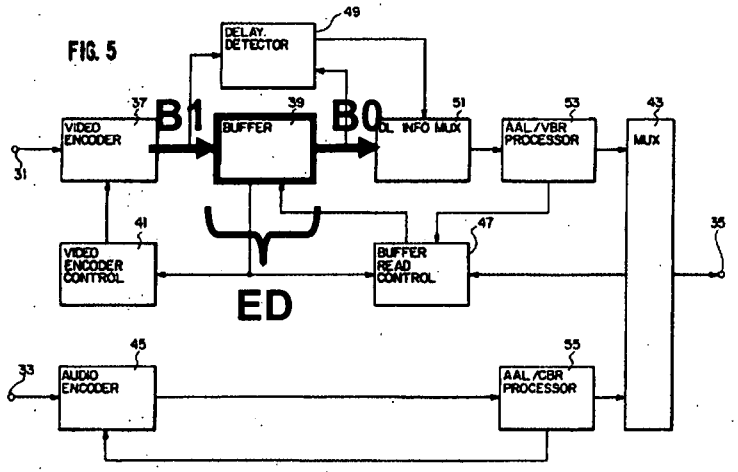


ED is " the delay in the buffer memory 39 of FIG. 5" (lines 16 and 17 of column 10) of Kiriyama



VD is "the additional video delay" (line 17 and 18 of column 10) and which is defined earlier at line 60 to 62 of column 9 to be "from the video buffer memory 71" and "relative to production of the separated video data from the video processor 65" (lines 59 to 62 of column 9)

The examiner's formulation of Equation (3) at page 6 of the examiner's answer is wrong. Condition (2) states a sum delay of the delay in the encoder buffer memory (ED) plus the additional video delay = THV. The derivation of ED is straight forward. The additional video delay is the delay in the decoder buffer (VD).However, the examiner states VD = B2 + B3 and then includes B2 + B3 and "an additional video delay" in Equation (3). In effect, counting the additional video delay (which is the decoder buffer delay) twice. NB: this is not material in the examiner's subsequent mathematical analysis



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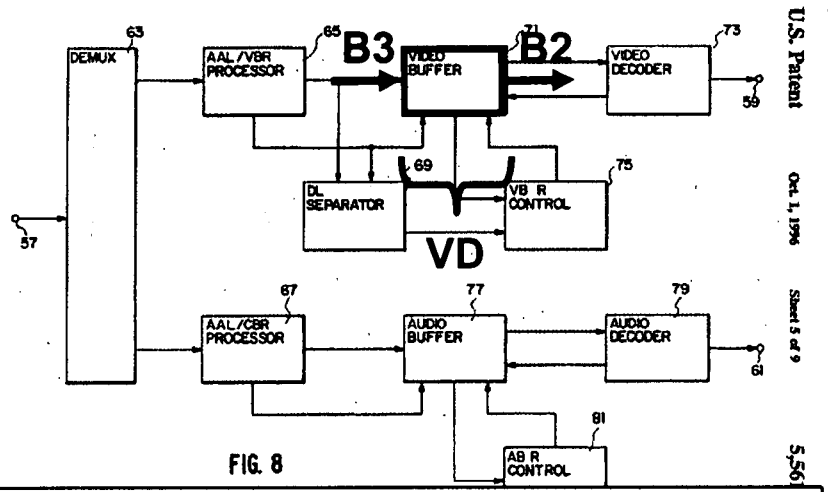

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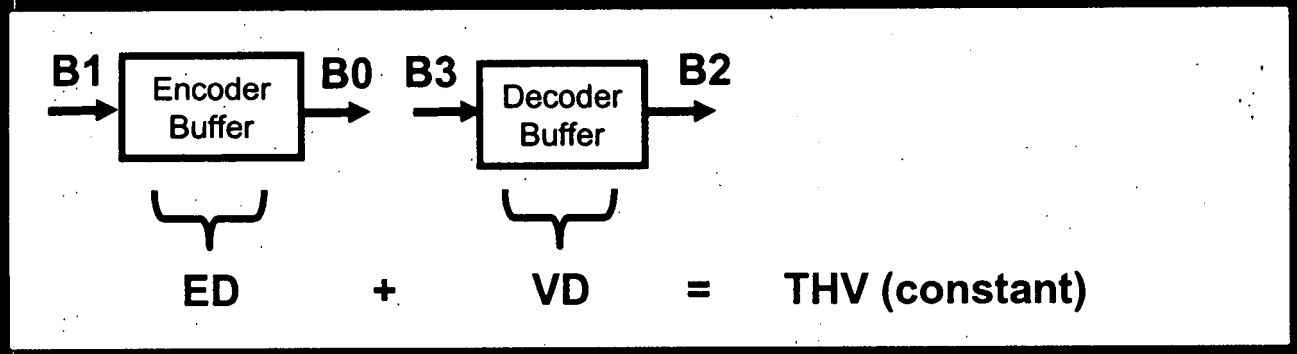
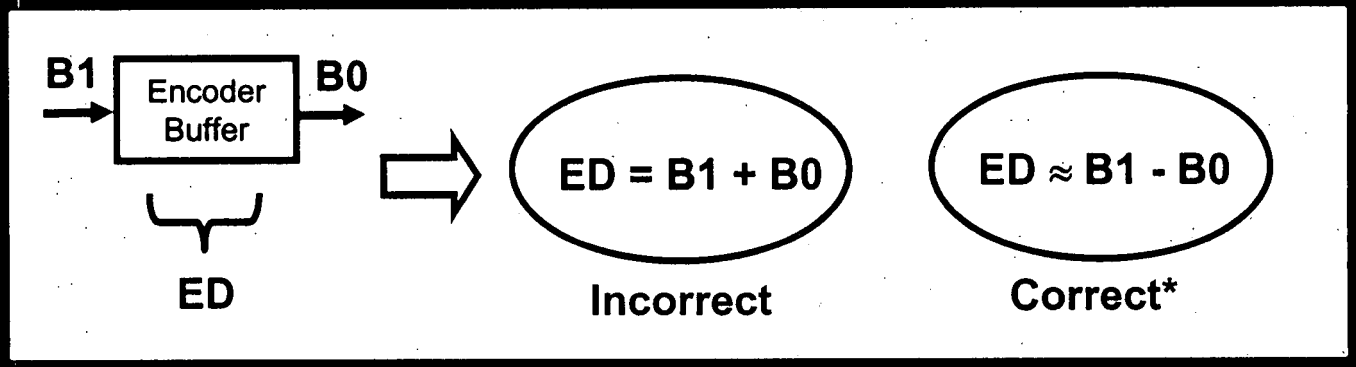
Taking the relevant bits,



The examiner is incorrectly suggesting that if ED + VD = constant, then changes in B1 must be inversely related to changes in B0, thus anticipating Keesman. In support of this, the examiner provides a mathematical explanation in the examiner's answer beginning on page 5.

In equation (1) on page 5 of the examiner's answer, the examiner is incorrectly suggesting that ED = B0 + B1:



* in fact, it is more correct to say ED is a function of B1 - B0 over time. I.e. ED = f(B1-B0, t)

The delay in the encoder buffer (ED) depends on the buffer occupancy and the rate at which the buffer is read out (B0). Also, the buffer occupancy is determined by the difference between the buffer input rates (B1) and buffer read out rate (B0) (i.e. B1 - B0) over time. All this is very basic, textbook buffer theory.

The incorrectness of the examiners statement can be illustrated by considering what happens if the buffer input rate (B1) remains constant and the buffer output rate (B0) increases. Obviously, the buffer occupancy will reduce and hence so too will the buffer delay (ED). However, based on the examiner's formulation of ED = B0 + B1, this would suggest that the delay (ED) increases if the buffer output rate increases which is absurd.

Based on the above and using an analysis similar to the examiners, we can equate the encoder buffer delay to be the buffer input rate (B1) minus the buffer output rate (B0):

$$ED = B1 - B0$$

Similarly for decoder buffer:

and $$VD = B3 - B2$$

Condition (2):

$$ED + VD = THV$$

Substituting for ED and VD gives:

$$B1 - B0 + B3 - B2 = THV$$ [and not examiner's B1 + B0 + B3 + B2 = THV - AVD]

Assuming no data loss, B0 = B3 and therefore cancel:

$$B1 - B2 = THV$$

I.e. one can not derive an inverse relationship between B1 and B0 from condition 2 of Kiriyama.